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Numerical study of a buoyancy-induced flow along a vertical plate with discretely heated integrated circuit packages

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Abstract—A numerical study by the multigrid technique has been performed to investigate the laminar natural convection air cooling of a vertical plate with five wall-attached protruding, discretely heated integrated circuit (IC) packages. This study is of great practical importance because it shows the influence of the blockages (IC package) dimension, and of their power distribution on the buoyancy-induced flow and thermal field in such a configuration. A two-dimensional, steady state model is used to describe the conjugate natural convection/conduction heat transfer. The fluid physical properties are assumed uniform except for the buoyancy terms which are computed using the Boussinesq approximation of Navier–Stokes equations. The development of the buoyancy-induced flow has been studied through the evolution of the streamwise velocity, temperature and heat flux fields. Copyright © 1996 Elsevier Science Ltd.

1. INTRODUCTION

Conjugate conduction/natural convection heat transfer is of high importance in many industrial applications, such as in cooling of electronic equipment. The current trend of miniaturization of electronic solid state devices has introduced problems of heat dissipation from the devices themselves. Although the total energy generated by a single electronic integrated circuit (IC) package is usually small (about 1.0 W), the chip surface area of the devices is so small that it induces a very high surface density of heat flux (currently higher than 1×10^5 W m^{-2}). Among the many possibilities for removing heat from an electronic device, that involve conduction, and/or convection (natural or forced) heat transfer, cooling with natural convection is considered as a cost effective and attractive technique because it is a convenient and inexpensive mode of heat transfer. Heat removal by this technique may be sufficient to keep weakly-heated electronic chips below a critical value set by reliability considerations.

During the last decade, engineers in the electronic industry have been looking for the best way to cool their electronic components. However, efficient cooling cannot be achieved without understanding the heat transfer from each specific component and determining the flow and thermal fields. It is in response to this need that simulations of cooling of electronic equipments have become active areas today, for experimental and computational research. Bar-cohen *et al.* [1] and Park *et al.* [2] have performed a thorough analysis of an energy balance system in order to describe the heat transfer process taking place in electronic equipments. Unfortunately, the analytical solution of this thermal balance system can provide heat fluxes and Nusselt numbers only for an ultra-simple configuration (smooth channel, uniform boundary conditions, no conjugate effect). Meanwhile, Sparrow *et al.* [3], Ortega *et al.* [4] and Garimella *et al.* [5] have investigated experimentally the effects of air cooling on an array of square heating elements protruding from the printed circuit board (PCB) in a three-dimensional, partially blocked channel. However, difficulty lies in performing the experiment for the poorly conducting heterogeneous IC packages (for instance, the epoxy type package), and in the long time required particularly for parametric studies. So, as complementary means, the influence of the IC packages in a channel on the flow and temperature fields has been studied extensively by numerical models (Habchi *et al.* [6], Afrid *et al.* [7], Shaw *et al.* [8] and Wang [9]). A rather complex situation has been investigated experimentally and numerically by Penot *et al.* [10], the velocity and thermal fields in enclosures containing many heat dissipating plates have been illustrated. The typical studies mentioned here all aim to provide a better physical interpretation or solution of

NOMENCLATURE

B	height of IC	T	temperature
C_p	specific heat of air	T_o	ambient temperature
e	board thickness	u	streamwise fluid velocity [m s^{-1}]
g	gravitational acceleration	v	transverse fluid velocity [m s^{-1}]
i	index relative to a given component	x	streamwise coordinate
L	streamwise dimension of IC	y	transverse coordinate
L_H	board height	z	third coordinate.
L_W	board width		
L_I	dimension of the inlet zone		
L_O	dimension of the outlet zone	Greek symbols	
L_G	streamwise dimension between the ICs	β	expansion coefficient
L_C	chip streamwise length	λ	thermal conductivity [W m^{-1} K^{-1}]
NC	number of components	λ_f	thermal conductivity of the fluid [W m^{-1} K^{-1}]
p	driving pressure		
p^*	total pressure	λ_s	thermal conductivity of the solid [W m^{-1} K^{-1}]
Q_i	heat dissipation of the ith IC [W]		
Q_{total}	total heat dissipation of the ICs [W]	μ	dynamic viscosity of air [kg m^{-1} s^{-1}]
q'	volumetric heat density [W m^{-3}]	ν	cinematic viscosity of air [m^2 s^{-1}]
q_i	flux surface density of the ith chip [W m^{-2}]	ρ	volumetric mass of air [kg m^{-3}]
		ρ_o	volumetric mass of surrounding air [kg m^{-3}]
q_m	mean flux surface density of the board [W m^{-2}]	ϕ	general variable.

the conjugate heat transfer phenomena associated with electronic equipment.

However, there are very few numerical contributions to the description, in a more realistic way, of the buoyancy-induced flow along a vertical plate with wall-attached protruding, discretely heated ICs. Moreover, the IC packages are considered here as obstacles, with the presence of the rather small size heated chip within the package, and the thermal conductivities of the different materials also taken into account. Hence, this article provides a more fundamental understanding of the influence of different characteristic parameters, such as the location of the greatest protuberance, the spacing between electronic components and the dissipated power distribution, on the velocity and thermal fields. Finally, this study represents an effort to employ the multigrid technique in the solution of the Navier–Stokes equations in conjunction with the energy equation for a conjugated problem.

2. PHYSICAL SYSTEM DEFINITION

Figure 1 shows the physical situation actually simulated, which was an array of five heated rectangular ceramic IC packages mounted on each side of a vertical electronic board. The boundary conditions and the location for which the results will be examined are also illustrated in Fig. 1(b). Table 1 summarizes the geometrical dimensions shown in Fig. 1 (a), (b), and the physical properties.

Table 1. Geometrical dimensions and physical properties of the reference case G

Symbol	Value	Symbol	Value
L_H [mm]	180	L_C [mm]	5
L_W [mm]	150	B [mm]	3
L_I [mm]	15	e [mm]	1.5
L_O [mm]	30	Q [W]	1.5
L [mm]	15	λ_S, PCB [W m^{-1} K^{-1}]	0.5
L_G [mm]	15	λ_S, IC [W m^{-1} K^{-1}]	15

From the point of view of the thermal and fluid conditions, the two sides of the vertical plate are assumed symmetrical. This assumption makes it possible to simulate just one of the two sides, by introducing an adiabatic condition along the middle of the vertical plate. When such a vertical plate with wall-attached protruding, discretely heated ICs, is placed in a sufficiently large electronic box (considered as the ambient condition), the steady cooling flow is induced along the vertical plate by virtue of the nonuniform density difference in the surrounding fluid.

The heat flux is calculated assuming a uniform heat distribution in the transverse direction, based on the board width L_W (see Fig. 1(a)), which is much greater than the height of the IC (B) and board thickness (e). This particular geometry allows the use of a two-dimensional, natural flow model, then the actual heat source Q_i (W) ($i = 1,2, \ldots NC$) on the chip NC_i which is assumed to be a very thin sheet almost without thickness, is transformed into a surface heat flux density q_i (W m^{-2}), given by:

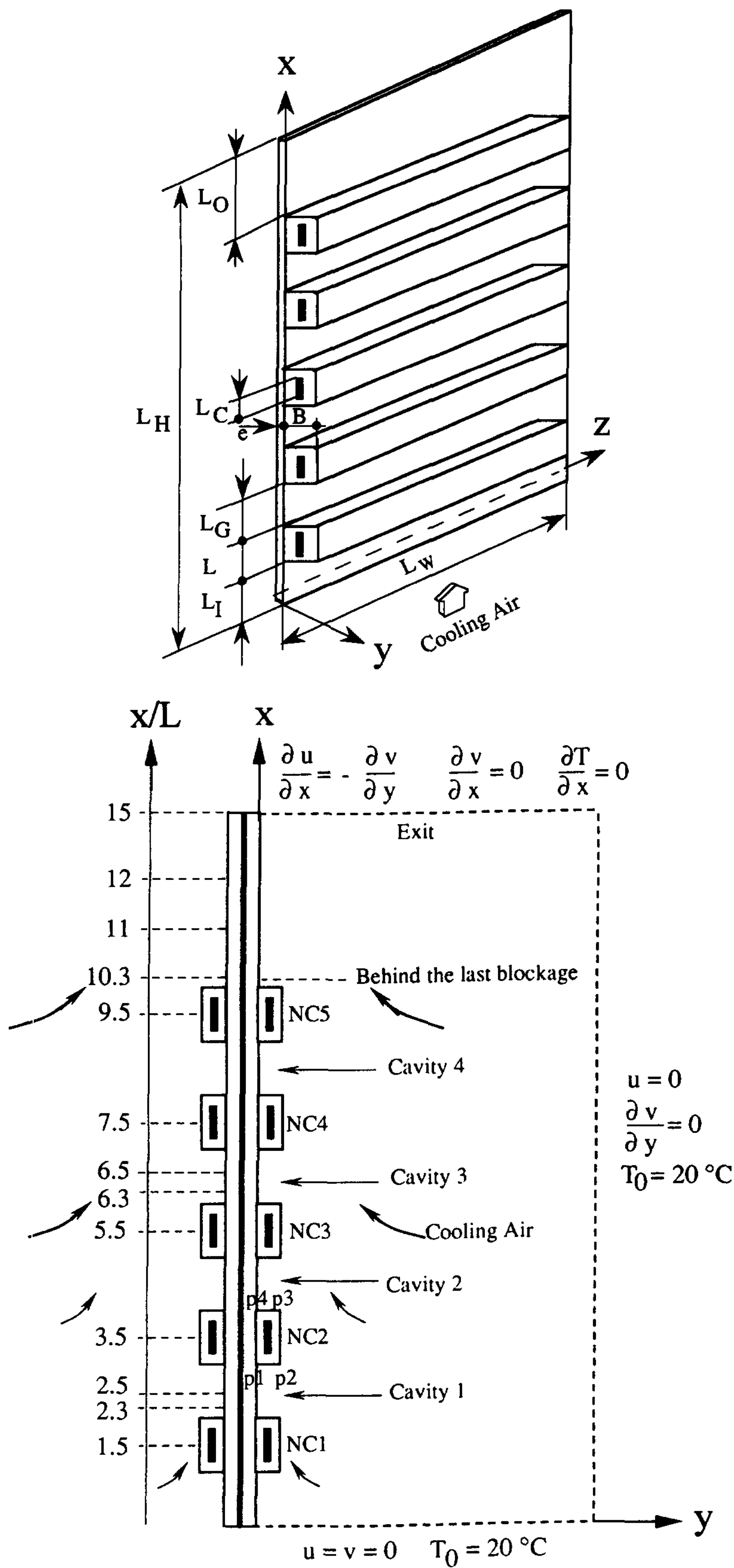

Fig. 1. (a) Simplified representation of the printed circuits board with five integrated circuit packages. (b) Description of the boundary conditions and the cuts across the board for examining the results at a given position (x/L).

$$q_i = \frac{Q_i}{L_W L_C}. \quad (1)$$

This heat is dissipated uniformly at a constant rate inside the junction region represented by the black layer in Fig. 1(a), (b).

The maximum Grashof number, defined as $Gr = (g\beta L_H^4 q_m)/v^2\lambda_f$ (here q_m is the mean value, $\Sigma Q_i/L_H L_W$, of the surface density) is about 10^9 corresponding to the total dissipated power of 7.5 W on a vertical plate with a width L_W of 150 mm, and a height of 180 mm, which is well below the critical value for turbulence (Gr of the order of 10^{10}). However, at the level of the IC package, the maximum of the local Reynolds number defined as $Re = uB/v$ (u is considered as a local velocity at the level of the IC) is about 10^2; the local Grashof number, defined as $Gr = (g\beta L^4 q_i/v^2\lambda_f$ is about 10^3, and the local ratio of Gr/Re^2 may be very small (about 10^{-1}). So the pure natural convection flow at the bottom may become mixed with the presence of a wake behind the IC package. Moreover, the buoyancy effect also retards the turbulent development. Accordingly, in spite of the protuberance of the ICs on the plate, the buoyancy-induced flow will globally remain laminar.

3. GOVERNING EQUATIONS

A two-dimensional, conjugate heat transfer, natural flow model is used for this study. Because of the presence of the thermal diffusion in the electronic board, and of the protruding, discretely heated IC package, the problem is elliptic in nature. All fluid properties are assumed uniform, and the fluid is assumed to satisfy the Boussinesq approximation which relates the temperature to the density through the following equation:

$$\rho = \rho_o[1-\beta(T-T_o)] \quad (2)$$

where ρ_o and T_o are the corresponding density and temperature of the surrounding, which is assumed to be isothermal and unstratified. Since a driving pressure $p(x)$ is defined as follows:

$$p(x) = p^*(x)+\rho_o g x. \quad (3)$$

Then the term $-(\partial p^*/\partial x)\rho g$ in the x-momentum equation becomes

$$-\frac{\partial p}{\partial x}+\rho_o\beta g(T-T_o). \quad (4)$$

With this background, the differential equations describing conservation of mass, momentum and energy can be written for the steady, laminar flow situation. The corresponding governing equations are as follows:

$$\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y} = 0 \quad (5)$$

$$\rho_o u\frac{\partial u}{\partial x}+\rho_o v\frac{\partial u}{\partial y} = -\frac{\partial p}{\partial x}+\mu\frac{\partial^2 u}{\partial x^2}+\mu\frac{\partial^2 u}{\partial y^2}+\rho_o\beta g(T-T_o) \quad (6)$$

$$\rho_o u\frac{\partial v}{\partial x}+\rho_o v\frac{\partial v}{\partial y} = -\frac{\partial p}{\partial y}+\mu\frac{\partial^2 v}{\partial x^2}+\mu\frac{\partial^2 v}{\partial y^2}. \quad (7)$$

A unique form is used to express the principle of energy conservation over the fluid and solid regions,

$$\rho_o C_p u\frac{\partial T}{\partial x}+\rho_o C_p v\frac{\partial T}{\partial y} = \lambda\frac{\partial^2 T}{\partial x^2}+\lambda\frac{\partial^2 T}{\partial y^2}+q'. \quad (8)$$

Here, q' (W m^{-3}) is the flux dissipated per unit of volume, and this equation holds over the entire computational domain, provided that in the solid region the fluid velocities are maintained equal to zero, which reduces the energy equation to pure condition. The thermal conductivities are set to λ_f in the fluid region, and to λ_s in the solid region. Moreover, the volumic source term q' in equation (8) is set equal to zero in the domains with no heat source.

4. NUMERICAL FEATURES

The finite volume forms of the above differential equations are derived by integrating them over discrete control volumes [11] in the physical domain. A staggered mesh system is used in which the discrete velocities are located on the faces of the finite volume cells and the discrete pressures and temperatures are situated at the cells centers. The finite volume equations, expressed per unit volume can be written in the general form:

$$a_P\phi_P - a_N\phi_N - a_S\phi_S - a_E\phi_E - a_W\phi_W = S_\phi\,\Delta x\,\Delta y. \quad (9)$$

The coefficients a_P, a_S ... and a_W represent the combined effects of convection and diffusion, and are obtained by using the Power-Law scheme. For laminar flows, conjugate conduction/convection heat transfer can be analyzed easily by using the harmonic averaging thermal conductivity at the interface between the solid and fluid. Sometimes, the ratio of the thermal conductivities of the materials (solid and fluid) may be as large as 10^3, and such treatment gives rise to very strong anisotropies in the discretized coefficients. This numerical difficulty has been efficiently solved through the Block Adjustment Procedure [12].

To solve the set of the finite volume equations, the boundary conditions have to be specified as shown in Fig. 1(b), which can be expressed as:

$$x = 0 \quad u = v = 0 \quad T = T_o$$

$$x = L_H \quad \frac{\partial u}{\partial x} = -\frac{\partial v}{\partial y} \quad \frac{\partial v}{\partial x} = 0 \quad \frac{\partial T}{\partial x} = 0$$

$$y \to \infty \quad u = 0 \quad \frac{\partial v}{\partial y} = 0 \quad T = T_o.$$

This means that at this location ($y \to \infty$), there is no shear and convection is the prevailing heat transfer mode. The truncated values of the infinity location in the y-direction can be increased until the variables become insensitive to further variation. In this study, the infinity value in the y-direction is equal to about $10B$. At the vertical wall:

$$y = 0 \quad u = v = 0 \quad T \quad \text{(unknown)}$$

$$y = -e \quad \frac{\partial T}{\partial y} = 0 \quad \text{(adiabatic condition)}$$

$$-e < y < 0 \quad u = v = 0 \quad \text{(solid region)}.$$

The fluid being isothermal away from the computational domain, the driving pressure is constant and maintained equal to zero.

For natural convection, due to the coupling between the velocity and thermal fields, the discretized dynamic and energetic equations (5)–(8) have to be solved simultaneously for u, v, p and T. In this procedure, called the smoother, we have retained the multigrid technique [13] to solve the equations (5)–(7) on each level of the grids, is the SIMPLEC algorithm [14]. The restriction to the coarse grid velocities is defined as the arithmetic mean of two neighbouring nodes in the fine grid, whereas we use the four neighbouring nodes for scalar variables. The prolongation operator is derived in all cases by using bilinear interpolation. The full multigrid procedure FAS-FMG [15], which starts at the coarsest grid and progresses in an adaptive manner to the finest grid, is appropriate. The multigrid technique has been applied to the analysis of heat transfer in electronic equipment [16] and detailed description of this method can be found in ref. [9].

5. RESULTS AND DISCUSSION

All the analyses were performed using our computer program, on a DEC3100 (about 15 Mips), running under UNIX. Case C (see Section 5.1. for the definition) of free convection cooling was solved with the finest level grids 61×65, 121×89 and 181×113, to determine the impact of the grid size in the convected flux, as shown in Fig. 2, along the vertical surfaces of the PCB and ICs. The velocity field was also examined,

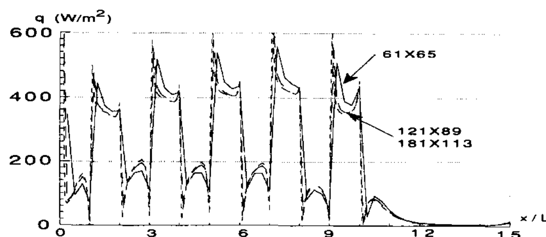

Fig. 2. Sensitivity of the convected flux to the grid size along all the vertical surfaces.

but is not presented here. It was found that the grid 121×89 practically reproduces the same convected flux and velocity field as the ones of the grid 181×113. So the nonuniform grid size 181×113 in a sequence of three grid levels, in which the coarsest grid size is 45×28, with a denser clustering near the solid structure was considered to give grid-independent results. The CPU time was then about 12 minutes for each tested case.

5.1. *Sensitivity study of heat transfer, to the location of the highest IC*

In this section, the influence of the location of the greatest protuberance on the flow and thermal fields will be discussed. In order to do this, the highest IC which is twice as high as the other small ICs, but has the same heat dissipation ($Q = 1.5$ W), was successively settled at the bottom (case A), the middle (case B) and the top (case C) of the vertical plate; the other ICs were smaller and geometrically identical, as defined in Table 1 for the reference case G (see Section 5.2).

5.1.1. *Velocity distribution.* The evolution of the streamwise velocity u along the vertical plate is illustrated in Fig. 3, and provides quantitative informations on the effects of the location of the greatest protuberance. It is shown that the development of the buoyancy-induced flow is essentially affected by the protruding, discretely heated blockages attached on the vertical plate, leading to an increase of the maximum velocity from 0 to 0.32 m s^{-1}. However, the influence of the greatest protuberance on the boundary layer flow remains rather localized just behind the highest blockage, as observed in the velocity profiles at $x/L = 2.3$, 5.5 and 10.3, respectively, for cases A–C. Beyond the greatest protuberance region, the buoyancy-induced flow rapidly joins the main streamwise flow downstream. Moreover, for the cases where the greatest protuberance is placed at the bottom (case A) and the middle (case B), the buoyancy-induced flow is maintained in a pure natural convection state all the way along the vertical plate. However, when the greatest protuberance is placed at the top (case C), a recirculating region appears just behind the last IC (negative velocity at $x/L = 10.3$); the flow separates beyond the last blockage, and reattaches further downstream on to the wall. That means the fluid flow in case C is progressively accelerated due to buoyancy along the vertical plate from a pure natural convection state at the bottom, up to a mixed convection regime near the top.

5.1.2. *Temperature distribution.* The influence of the localization of the highest IC on the temperature distribution along the line passing through the chips can be observed in Fig. 4. In all cases A–C, the difference of the chips temperature between the first and second ICs is remarkable; away from the inlet region, the increase of the maximum temperature remains rather moderate. An analogous analysis of the heat exchange as the reference case G (see Fig. 7(d)) in

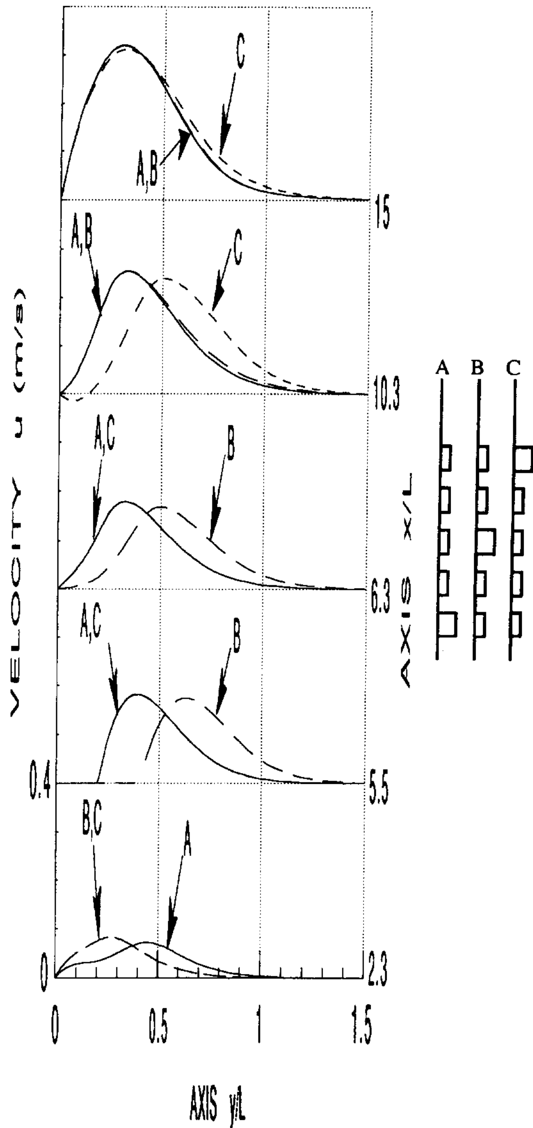

Fig. 3. Evolution of the streamwise velocity as a function of the greatest IC location.

Section 5.2.2. allows us to understand the effects of the highest IC on the chips temperature.

This is due to the fact that as the buoyancy-induced flow approaches the first heated blockage, the cold fluid flow is strongly deflected, and therefore, it directly transports about 65% of the power dissipated

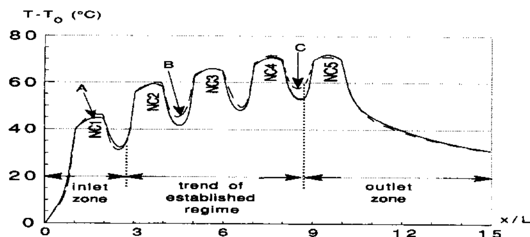

Fig. 4. Evolution of the chips' temperature as a function of the greatest IC location.

by the first IC into the surroundings. Then, the strong energy accumulation due to the power unloaded by the first IC, rapidly leads to a less efficient heat transfer for the second IC, as evidenced by a significant increase of its temperature.

These remarks also apply for the other ICs, and each of them is surrounded by the same kind of open cavity flow (see Fig. 1(b)) between the ICs, signifying similar heat exchange conditions: if about 65% of the power dissipated by each IC (1.5 W) is still directly convected into the air, 35% is, at first, injected in each such cavity through the conjugate effect between the solid and fluid, then exchanged with the core flow through the cavities which have actually an active contribution to the cooling. Correspondingly, this similar heat exchange surrounding induces a smooth growth of the chip temperature between the neighbouring ICs (*NC*3-5).

Although, the presence of the highest IC locally modifies the velocity field, the value of the chips temperature is practically insensitive to the location of the highest IC. It is also noted that the convected flux from the surface *p*3*p*4 (see Fig. 1(b)) of the second cavity decreases to 3.5% Q_{total} in case B, instead of 4.3% Q_{total} in cases A and C. A similar trend is found for the fourth cavity in case C, the flux decreases to 2.7% Q_{total}, instead of 3.7% Q_{total} in cases A and B. This is due to the increasing blockage effect of the highest protuberance on the boundary layer flow, leading to a less efficient heat exchange there.

5.2. *Sensitivity study of heat transfer to the spacing between the ICs*

The effects on free convection of a variation of the streamwise spacing L_G between the ICs are investigated here. Numerical studies are always performed for a vertical plate with a given height, supporting five uniformly heated ICs (1.5 W per IC). Four configurations are considered, with different values of the spacing range, characterized by $L_G/L = 0$, 0.25, 0.5 and 1, identified respectively by the symbols D, E, F and G. Note that the first IC is always located at the same elevation L_I (see Fig. 1).

5.2.1. *Velocity distribution.* The velocity profiles across the section at the middle of each cavity, just downstream of the last IC, and at the exit are compared in Fig. 5. It is first observed that the value of the maximum velocity in the core flow is insensitive to variation in L_G. Figure 5 shows that for $L_G/L = 0.25$ and 0.5, the fluid in the open cavity is almost stagnant, as evidenced by a relatively small velocity value. However, at $L_G/L = 1$, the cavity is filled up with the buoyancy-induced flow, resulting in a significant local increase of the streamwise velocity. The buoyancy-induced mass flow rate decreases from cases D–G, which is clearly shown by the difference in the axial velocity at the exit. This is due to the fact that the buoyancy effects on the flow, relative to the higher level of the chips temperature in case D (see Fig. 6), are more important, and moreover, the pres-

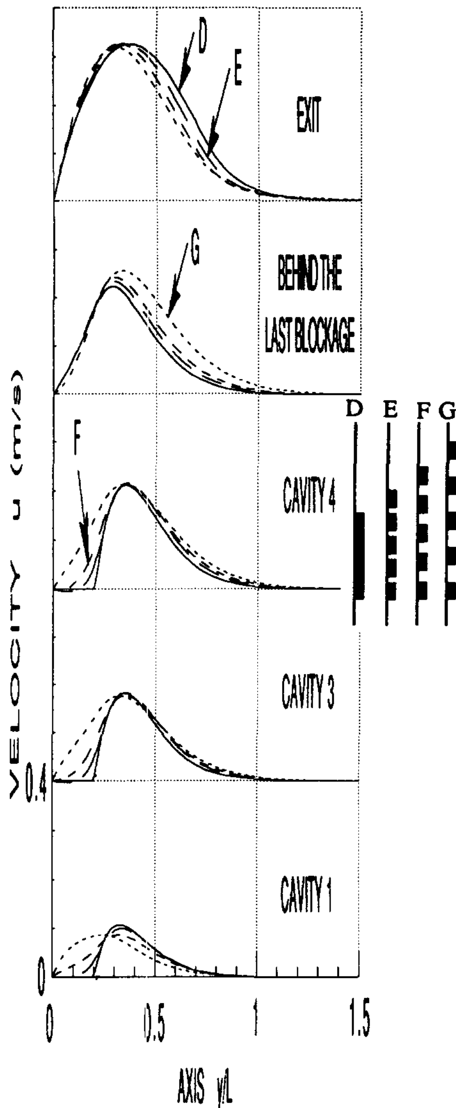

Fig. 5. Evolution of the streamwise velocity profiles as a function of the spacing L_G/L.

sure drop in case D is the minimum because of a smaller wall roughness.

5.2.2. *Temperature and heatline distributions.* For the conjugate heat transfer, the heat exchange between the heated ICs and cooling fluid is associated directly with the distribution of blockages. The transport of energy through the flow field is a combination of both

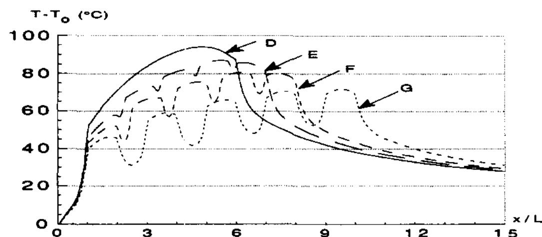

Fig. 6. Evolution of the chips temperature as a function of the spacing L_G/L.

thermal diffusion and enthalpy flow. A heat function H proposed by Bejan [17] is used for the analysis of heat exchange, and defined as:

$$\frac{\partial H}{\partial y} = \rho_o CpuT - \lambda f \frac{\partial T}{\partial x}$$

(net enthalpy flow in the x direction)

$$-\frac{\partial H}{\partial x} = \rho_o C_p vT - \lambda f \frac{\partial T}{\partial y}$$

(net enthalpy flow in the y direction).

In the heatline pattern visualization, the interval between the heatlines, referred to by the integer numbers 1–9, signifies an energy corridor, along which the heat production from the ICs dissipation is transported by the fluid flow. The real number represents the value of the flux (W) loaded by the fluid flow from the inlet/outlet zones, and around each IC ($p1p2p3p4$, see Fig. 1(b)). Also indicated is the value of the conductive flux (W) at the interface ($p1p4$) between the heated ICs/PCB. The analysis of energy corridor, for example, between the heatlines 8–9 in Fig. 7(a) attached to and then leaving the first IC (NC1), allows us to understand the variation of the chips temperature with the different distribution of the ICs.

The temperature and heatlines pattern are illustrated by Figs. 6 and 7 and it is shown that the spacing between the ICs has an important influence on the chips temperature level, and the heatlines distribution. When the spacing between the ICs approaches zero ($L_G/L = 0$), the chips temperature rises rather strongly from the first to the last ICs. The fact of assembling the five discrete ICs into a single heated element leads to a significant increase of the chips temperature for the five ICs, compared to that of other cases. This can be explained because the contact between the ICs enhances the conductive exchange through the interfaces $p1p2$ and $p3p4$: the first IC is, for instance, able to directly collect 20% (according to the direction sign in Fig. 7(a)) of the power dissipated by its downstrean neighbour; however, the power collection towards upstream progressively decreases from 13 to 7 to 1.3% for the second, third and fourth IC, respectively. As a consequence, a stronger accumulation of energy at the inlet zone results in a rapid decrease of the exchange efficiency there, which is responsible for the higher chips temperature downstream.

When the spacing between ICs is not equal to zero ($L_G/L \neq 0$), this streamwise temperature gradient remains; however, it is much less marked. Moreover, the chips temperature decreases with the increase of L_G for all the ICs. This is due to the fact that as the ICs are progressively distributed along the vertical plate, the energy accumulation in the outer 'energy corridor' from the heatlines 8 in case D and 9 in case G, attached to inlet zone (PCB leading edge and the two first sides $p1p2$ and $p2p3$ of the first IC) decreases from 26% Q_{total} in case D to 18% Q_{total} in case G. When increasing L_G, the flux density to be convected

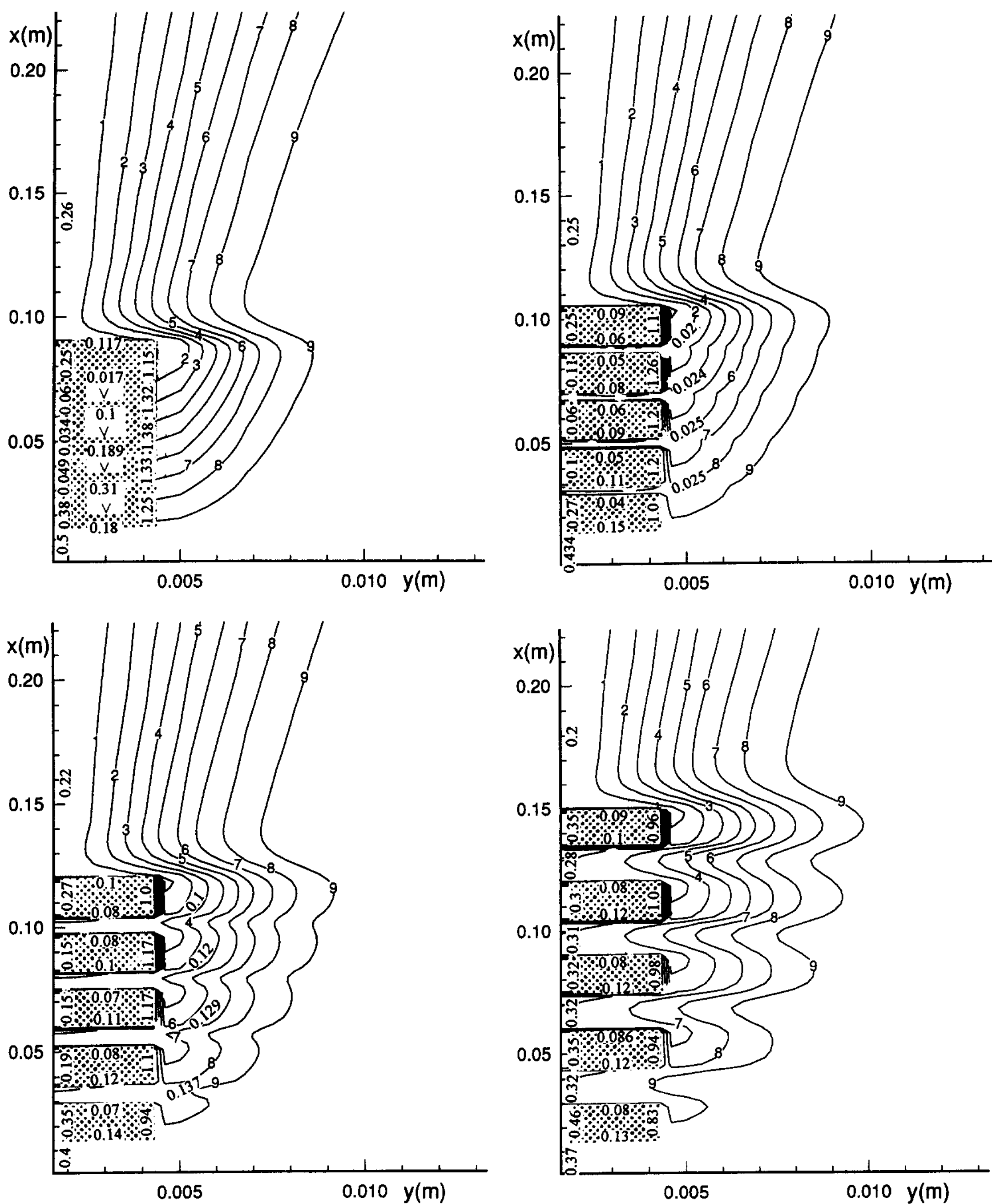

Fig. 7. Heatlines pattern as a function of the spacing L_G/L: (a) case D ($L_G/L = 0$); (b) case E ($L_G/L = 0.25$); (c) case F ($L_G/L = 0.5$); (d) case G ($L_G/L = 1$).

by the part of the PCB located around a given IC decreases; and the convective exchange, for example, between cavity 1 (see Fig. 1(b)) and the core flow, increases from 0.025 W in case E, to 0.137 W in case F and to 0.32 W in case G between heatlines 8 and 9. A similar trend for the other cavities, 2–3, which become more and more active for convective exchange with the increase of L_G, is also observed.

5.3. *Sensitivity study of heat transfer to heat input distribution*

In practice, the electronic components might dissipate different power. In this section, nonuniformly heated arrays, corresponding to cases H, I, J, and K, are investigated. Case G with a uniformly heated array, but for the same total dissipated power (7.5 W), is considered as a reference for the comparison

with the other cases H–K. Let us define the non uniform configuration as:

- ascending in case H;
- descending in case I;
- ascending–descending in case J;
- descending–ascending in case K.

The schematic of the heat input distribution and its value are shown in Fig. 8.

5.3.1. *Velocity distribution.* The velocity profiles across the characteristic sections of the vertical plate ($x/L = 2.5$, 6.5, 11 and 15) are plotted in Fig. 9. Although, in all cases H–G, the flow is induced by buoyancy with the same dissipated power ($\Sigma Q_i = 7.5$ W), the influence of the power distribution on the velocity profiles is relatively strong. When most of the power is dissipated at the bottom of the plate (case I), a bigger mass flow rate is produced due to the stronger buoyancy effects there, as evidenced by the higher velocity at $x/L = 2.5$. Consequently, this flow in case I maintains this advantage along the vertical plate, as shown with a higher velocity at the exit ($x/L = 15$). On the contrary, when the weakly heated ICs are settled in the inlet zone (case H), the buoyancy-induced flow is weaker, as observed with the lower velocity at $x/L = 2.5$, and then accelerated more and more strongly, up to practically the same maximum velocity as that in case I, but with a relatively smaller mass flow rate. Figure 9 also shows that similar trends in the velocity profiles are observed for the power distributions of ascending-descending case J, and of descending-ascending case K but they look similar:

- between cases H and J at the bottom;
- between cases I and K also at the bottom;
- and between cases J, K and G at the top.

5.3.2. *Temperature and heatline distributions.* A comparison of the chips' temperature given in Fig. 10 shows that the difference of the maximum temperature among cases G–K is significant, when distributing the total dissipated power (7.5 W) in the different manners, as described in Fig. 8. If case G in which uniform input distribution is considered as a reference,

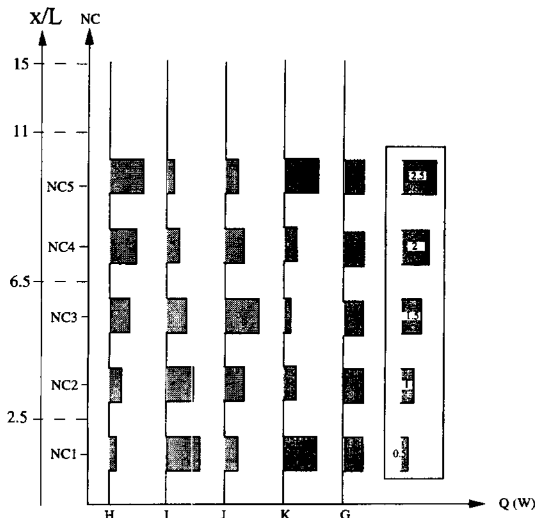

Fig. 8. Schematization of the heat input Q distribution.

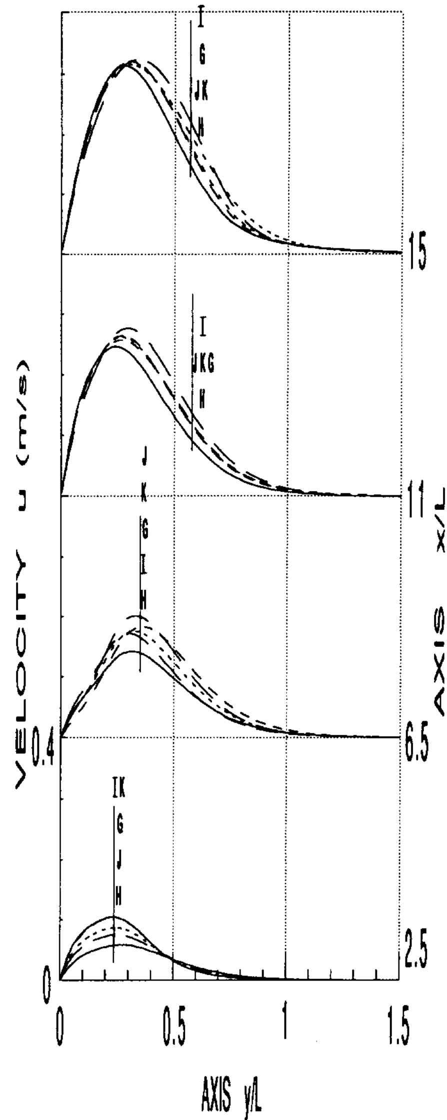

Fig. 9. Evolution of the streamwise velocity profiles as a function of the heat input Q.

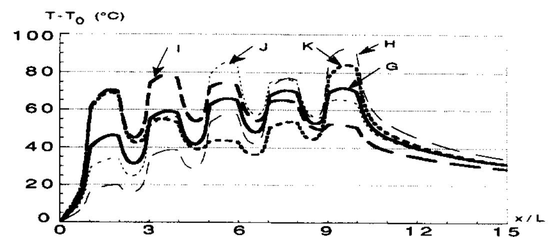

Fig. 10. Evolution of the chips temperatures as a function of the heat input Q.

we observe that the maximum temperature significantly increases:

- by as much as 23°C for the ascending distribution (case H);
- by only 6°C for the descending distribution (case I);
- by, respectively, 15°C and 13°C for the ascending–descending distribution (case J) and for descending–ascending one (case K).

Clearly, the uniform power distribution gives the lowest maximum temperature.

The heatlines patterns, defined in Section 5.2.2, for the nonuniform power distributions (cases H–K) are also presented in Fig. 11. It can be seen that in case G, the uniform power distribution (see Fig 7(d)) gives the most regularly increasing enthalpy rate. Let us also observe that the outermost 'energy corridor' from heatline 9, corresponding to the inlet region transports, in case G, about 18% of the total dissipated power. In case H (see Fig. 11(a)), only 6% of the total dissipated power is transported in the inlet region, whereas the convected flux into the 'energy corridor'

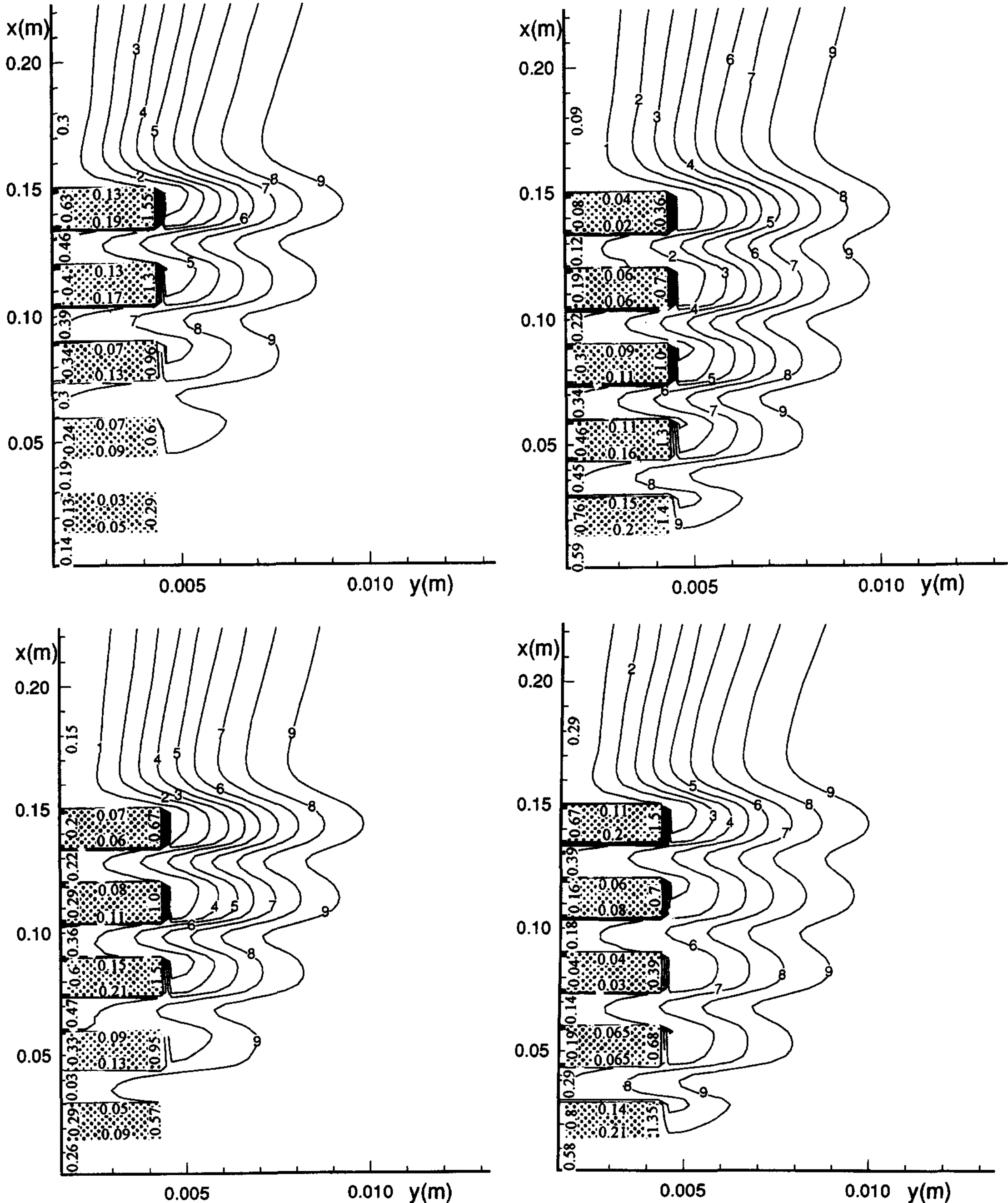

Fig. 11. Heatlines patterns as a function of the heat input Q: (a) case H (ascending); (b) case I (descending); (c) case J (ascending–descending); (d) case K (descending–ascending).

between heatlines 1–4 attached to the last IC increases up to 25% of the total power. However, the heat exchange efficiency progressively decreases downstream, thus the stronger power dissipation of the last IC can not be efficiently evacuated, leading to a significant increase of the chips' temperature from the first to last IC, which is also the hottest in all cases H–G. On the contrary in case I, when the strongly heated IC is settled in the inlet zone, the outer 'energy corridor' from heatline 8 (see Fig. 11(b)) attached to the inlet zone transports almost 29% of the total dissipated power thanks to an efficient convective exchange there. Yet with this 'energy corridor' being already much loaded, it has a rather negative behaviour in the following ICs, and particularly on the second one, which is still dissipating a high power.

The analysis is a bit more complicated when dealing with the non-monotonous distribution of power, such as in cases J and K. The heatlines distribution of case J shown in Fig. 11(c)), presents a strong concentration of energy between heatlines 5–7 in the central part of the board, at which the IC with the bigger power (about 1/3 of the global dissipation) is installed. The hotter wake around this central IC clearly induces a blocking effect for heat exchange on the following ICs which dissipate a relatively smaller power, but yet have the high temperature value. The last configuration with a descending-ascending distribution (case K) leads to a mapping of heatlines, shown in Fig. 11(d), which is of course very similar to that of case I at the level of the first IC (the same dissipated power). The discussion becomes interesting when comparing the behaviour of the upper most IC among cases K and H. In fact, the thermal load of the fluid is very similar in each of the cases, but the velocity field is different. The velocity is a bit higher in case K, and as a consequence, the diffusion of the heat is also more important: the air is less hot when arriving at the level of the last IC, and thus its temperature is lower in case K. It is seen also that when a strongly dissipative IC is not surrounded by other big heat sources, the conduction at the interface $p1p4$ between the heated IC and PCB increases, and the board contributes also to cool this IC (see the last IC in case K (0.67 W)) in comparison with that in case H (0.63 W), or the central IC in case J (0.6 W).

6. CONCLUSIONS

The cooling by free natural convection, of integrated circuit packages mounted in a vertical board has been studied by using an efficient multigrid technique. The influence of the geometrical parameters (B and L_G), and of the dissipated power (Q) on the velocity and temperature fields has been shown, and the main trends can be summarized as follows. Concerning the sensitivity to geometrical parameters (B and L_G), it is observed that the fact of uniformly distributing the ICs along the electronic board results in a lower chip temperature, as compared to that of assembling all the ICs in the inlet zone. However, the maximum temperature is found to be insensitive to the position of a bigger component along the electronic board. In general, there is a large interval in the chips' temperature between the first and second ICs, then this increase is very moderate downstream. For the buoyancy-induced flow, the perturbation of the boundary layer flow due to the different distribution of the heated ICs, remains very localized, and does not propagate far away. Moreover, the buoyancy-induced mass flow rate is practically insensitive to the variation of the geometrical parameters.

The sensitivity study has also been performed by keeping the same global power dissipated by ICs, but with different power distributions along the board. The prediction clearly shows that the uniform power distribution is the best case, and leads to the lowest maximum temperature. Also, if one of the ICs is highly dissipating, its best location is in the inlet region of the board. In all cases, the buoyancy-induced flow is starting in a purely natural convection in the bottom of the board, but develops to a mixed one in the top, where a small recirculation zone appears behind the last IC. Finally, all these results are given for a free convection environment, and an interesting complementary study could be developed for confined or thermally stratified configurations.

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